AMENDMENT

In the specification:

Page 6, paragraph 3:

A sectional view of an interconnect layer 30 of an integrated circuit chip is shown in FIG. 10, and includes a low-k dielectric material including a via dielectric layer 31 and a trench dielectric layer 32 formed over an underlying interconnect layer 33 having a conductive metal 34. An insulative barrier layer 35, usually comprising silicon nitride or silicon carbide, is first deposited over the underlying metal layer 33 which includes a barrier layer 35 formed over a conductive interconnect layer 33.

Please amend the claims as follows:

Please cancel claims 1-5, without prejudice.

6. (Currently amended) A method of forming a dual damascene interconnect structure of an integrated circuit device, said interconnect structure having a low-k dielectric material deposited over an underlying metal layer, comprising the steps of:

a. forming a passivation mask film over the low-k dielectric material;

b. forming a barrier mask film over the passivation mask film;

c. forming a metallic mask film over the barrier mask film, and said passivation film and metallic mask films forming a mask layer overlaying